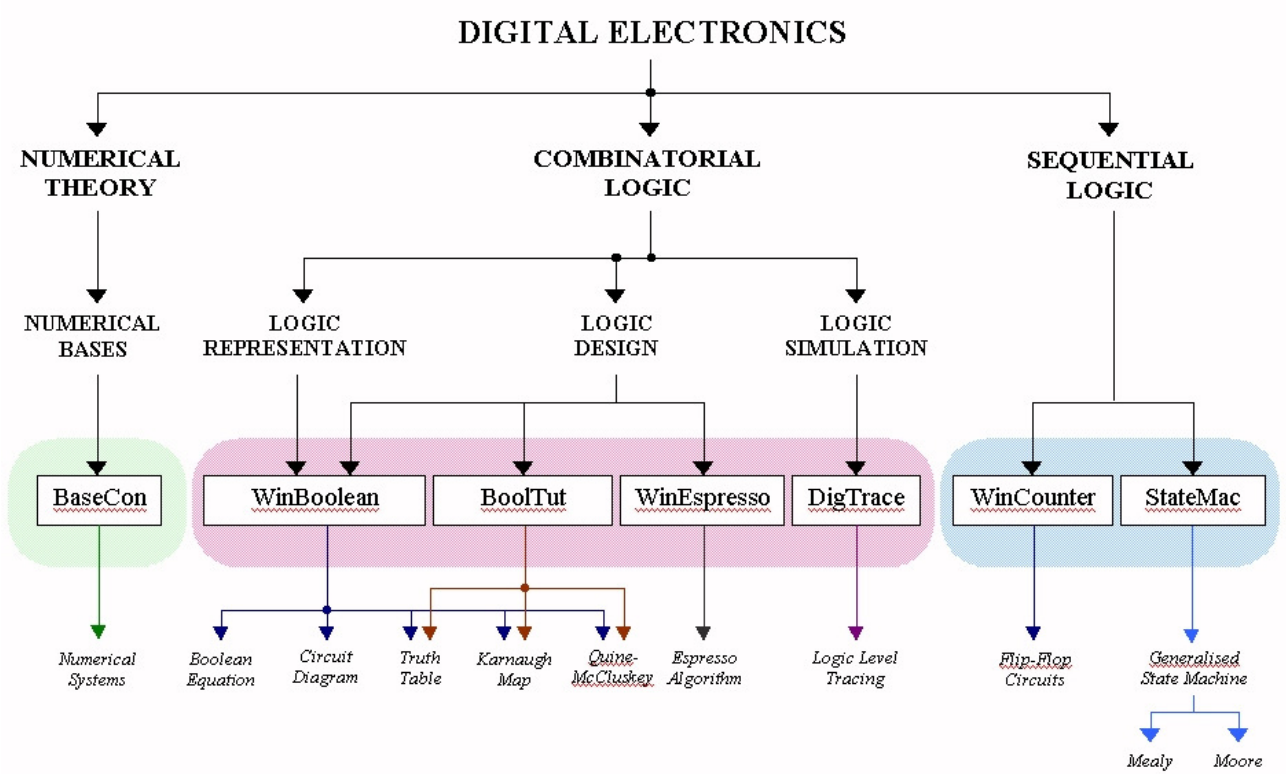
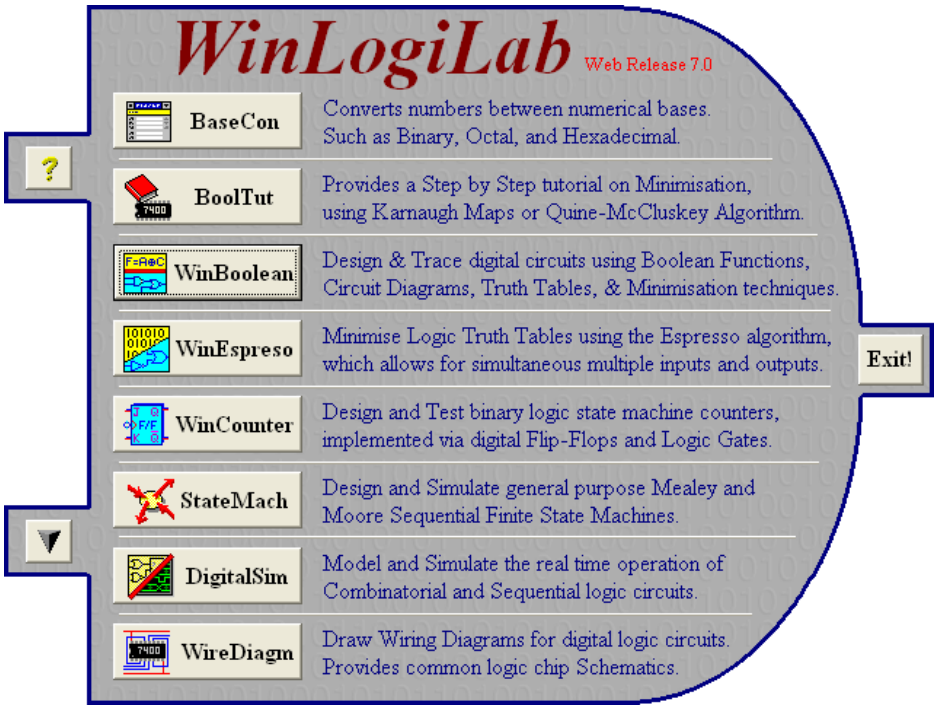
WinLogiLab

Rev. Jan 08

Følgende viser strukturen i WinLogiLab.



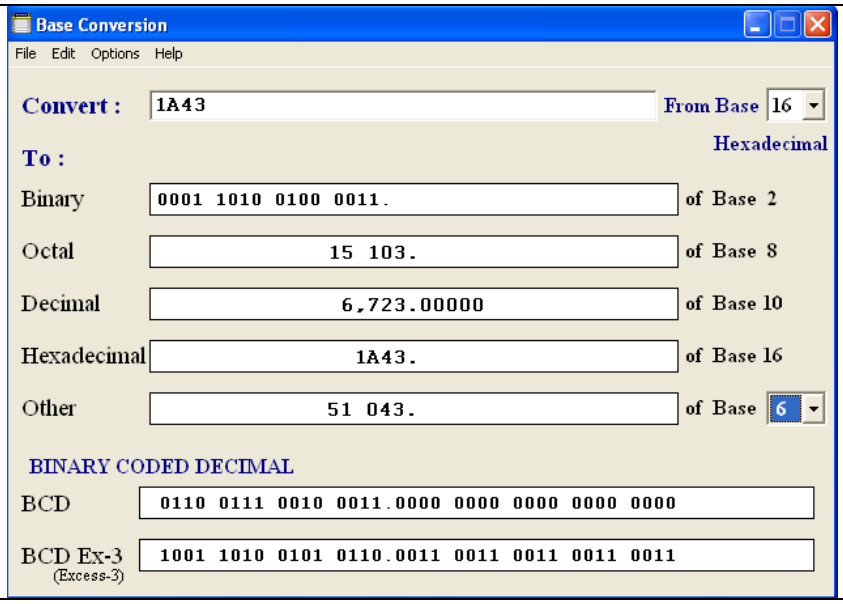
Startbilledet, hvorfra man vælger de forskellige del-programmer i systemet.



På de følgende sider er der vist en slags træstruktur. I venstre søjle ses programdelen. Og til højre herfor nogle skærmbilleder for nogle af de muligheder, der er i pågældende delprogram.

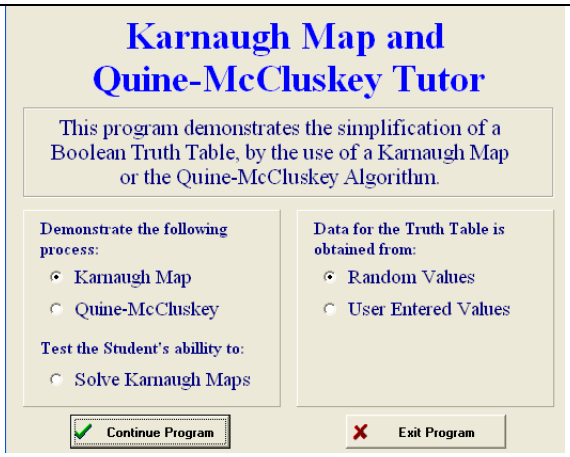
BaseCon

I denne programdel fås en omfattende base-konverter.



BoolTut

Programdelen er en tutorial i reducering af boolske ligninger vha. karnaugh kort.

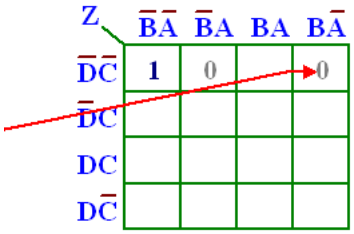


Programmet kan øve / forklare karnaugh-kort minimering.

Skal man bruge programmet til reducere karnaughkort, klik i

Man kan angive output. Kan enten være 0, 1 eller X (Don't care)

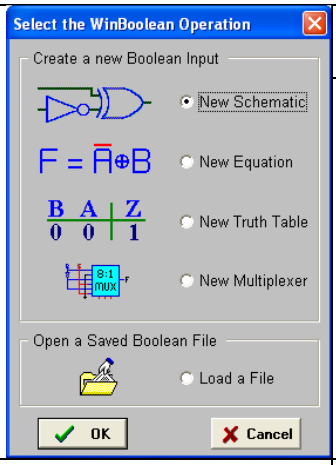
DEC	NUM ONES	INPUTS D	C	B	A	OUTPUT Z
0	0	0	0	0	0	1
1	1	0	0	0	1	0
2	1	0	0	1	0	0
3	2	0	0	1	1	1
4	1	0	1	0	0	1
5	2	0	1	0	1	X
6	2	0	1	1	0	X
7	3	0	1	1	1	X
8	1	1	0	0	0	1
9	2	1	0	0	1	1
10	2	1	0	1	0	1
11	3	1	0	1	1	0
12	2	1	1	0	0	0
13	3	1	1	0	1	1
14	3	1	1	1	0	1
15	4	1	1	1	1	1



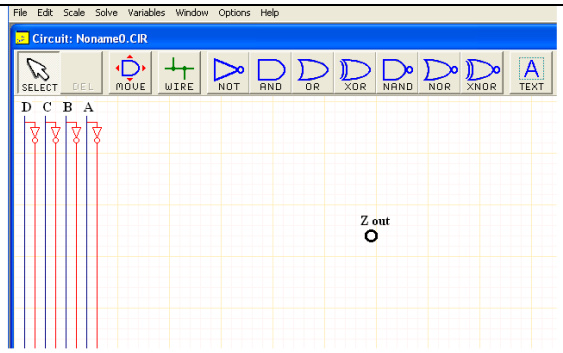
Nu skal man klikke sig gennem programmet, og man lærer hvordan det sker !!

WinBoolean

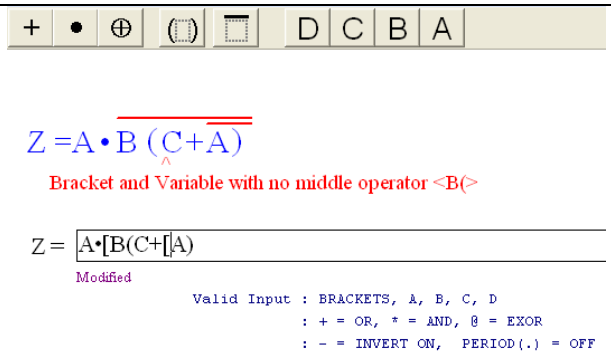
Denne pro-gramdel har flere under-dele.



Vælg indgang. Hvad er det, der er udgangs-situationen ??



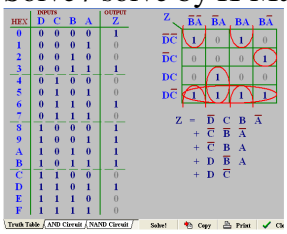
New equation input



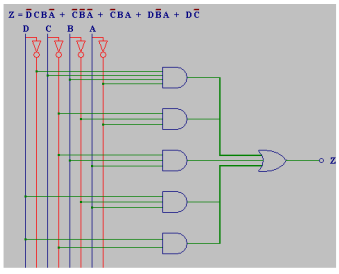
New Truth table

DEC	NUM ONES	INPUTS D	C	B	A	OUTPUT Z
0	0	0	0	0	0	1
1	1	0	0	0	1	0
2	1	0	0	1	0	0
3	2	0	0	1	1	1
4	1	0	1	0	0	0
5	2	0	1	0	1	0
6	2	0	1	1	0	1
7	3	0	1	1	1	0
8	1	1	0	0	0	1
9	2	1	0	0	1	1
10	2	1	0	1	0	1
11	3	1	0	1	1	1
12	2	1	1	0	0	0
13	3	1	1	0	1	1
14	3	1	1	1	0	0
15	4	1	1	1	1	0

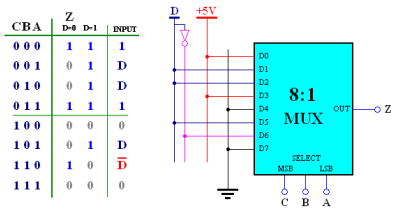
Solve / solve by K-Map



Vis AND eller NAND løsning

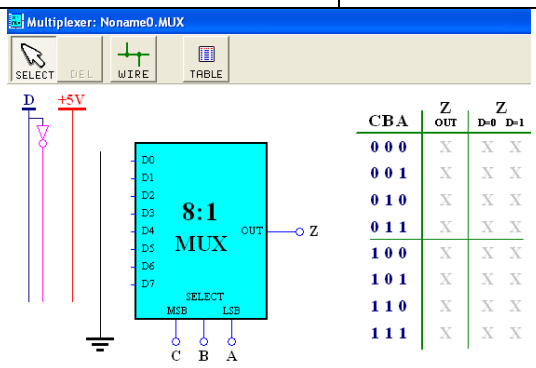


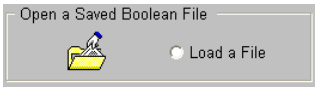
Solve / Solve by mux



New Multiplexer

Her kan man lave reducering af boolske ligninger vha. en MUX.



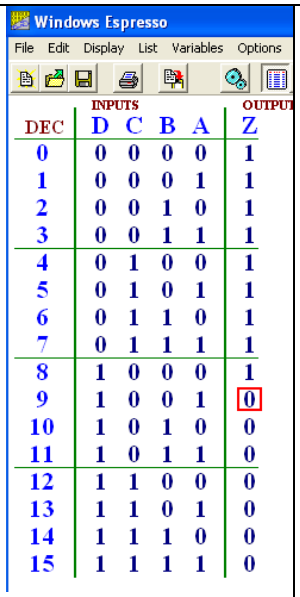


Der er mulighed for at gemme ????hvor ????? og genloade en ligning ???

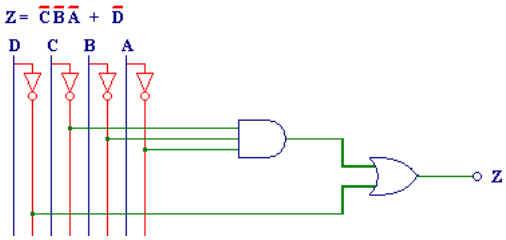
WinEspreso

I WinEspreso går man fra sandhedstabel til diagram.

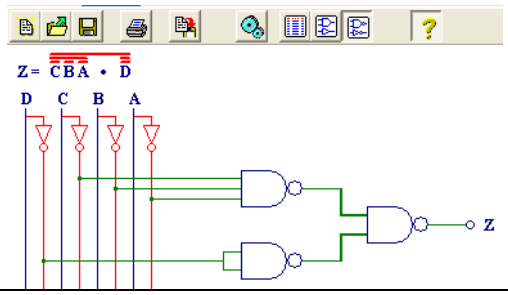
Diagrammet kan omformes til NAND-gates.



Minimize, tryk 

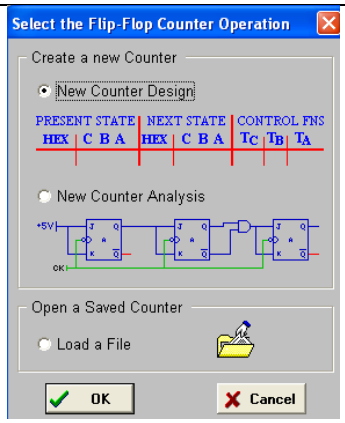


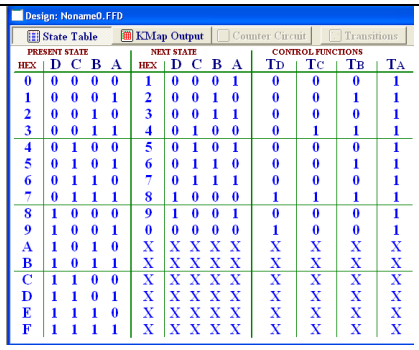
Tryk på  for at tegne NAND-gate kombination.



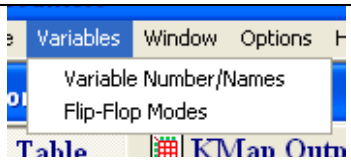
WinCounter

Her kan man lave design af tællere.

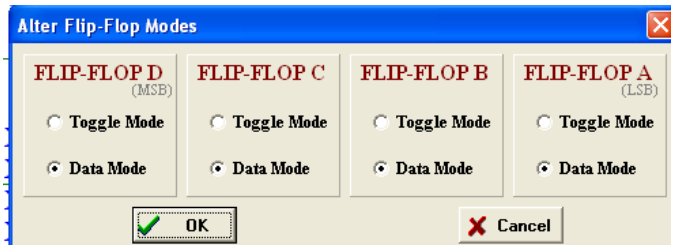


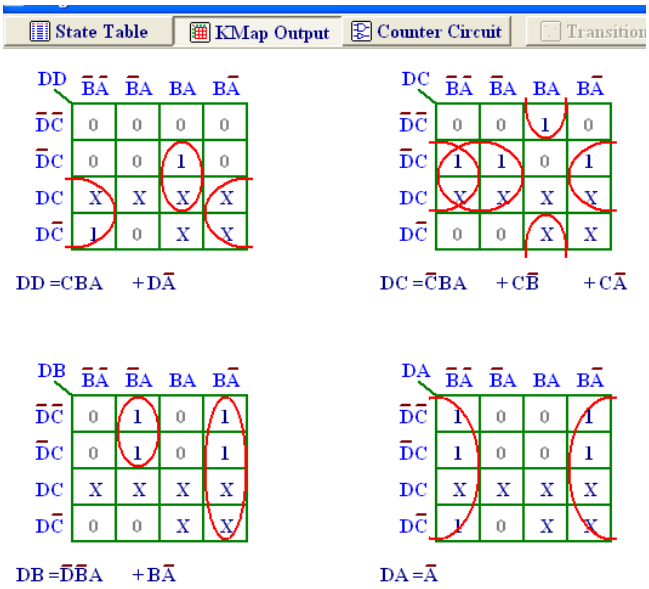


Vælg

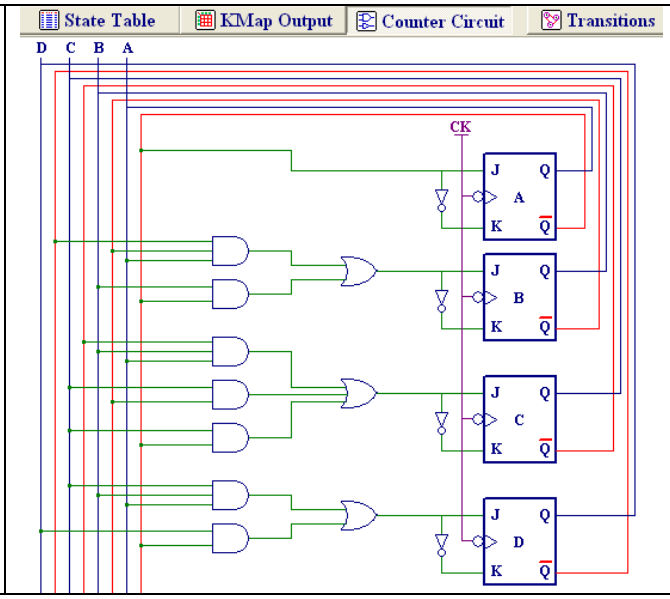


Der kan vælges D-Flip Flops for alle eller nogle af FF-erne.





Efter karnaugh kort design, tegnes kredsløbet.



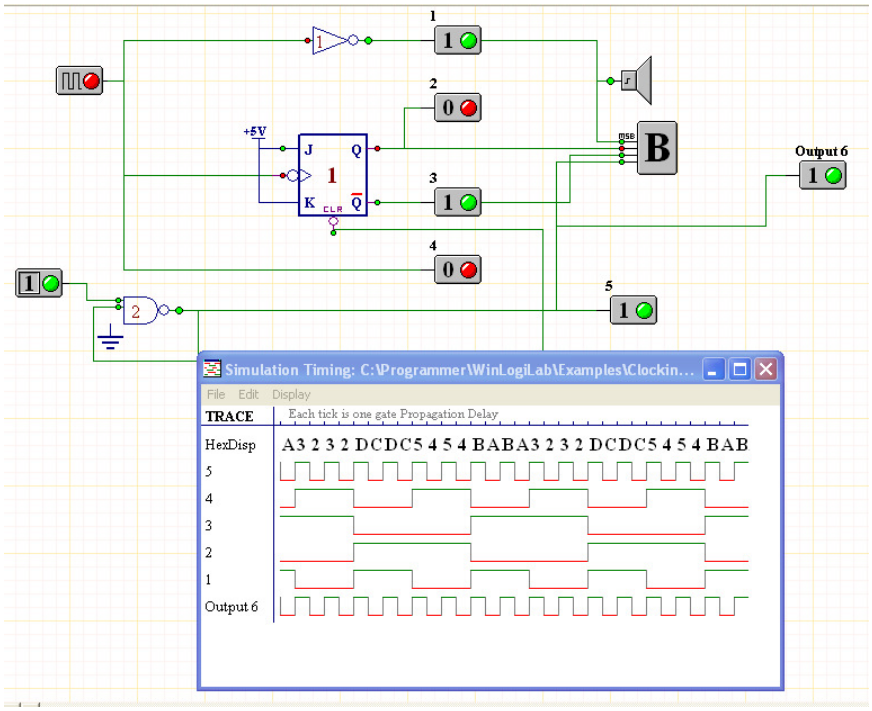
StateMach

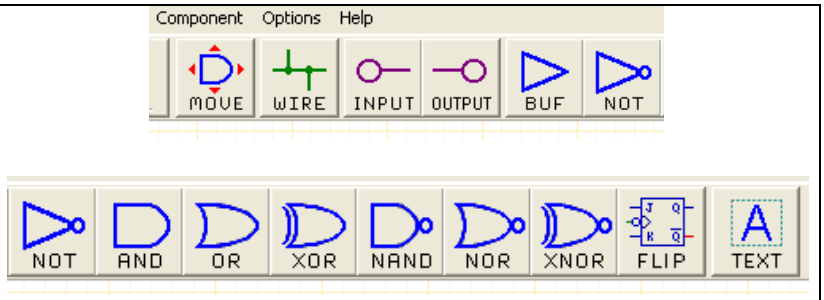
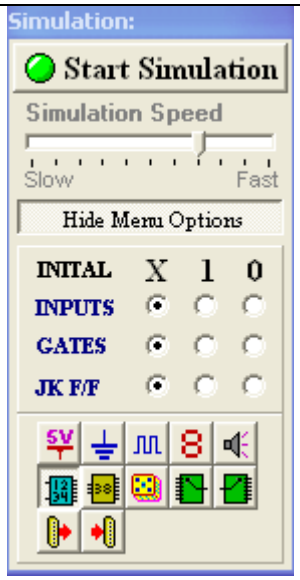
???????

DigitalSim

Denne del er genial til at tegne digitale kredsløb og simulere dem.

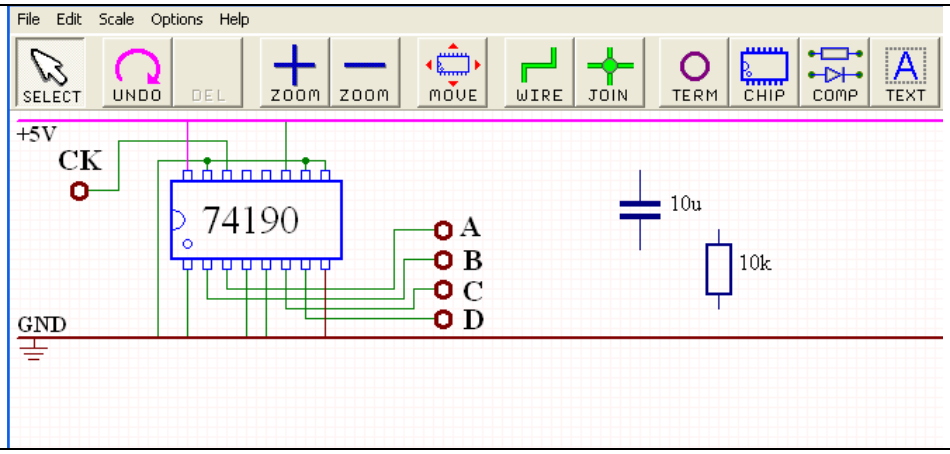
Eksempel på et kredsløb fra det medfølgende bibliotek:



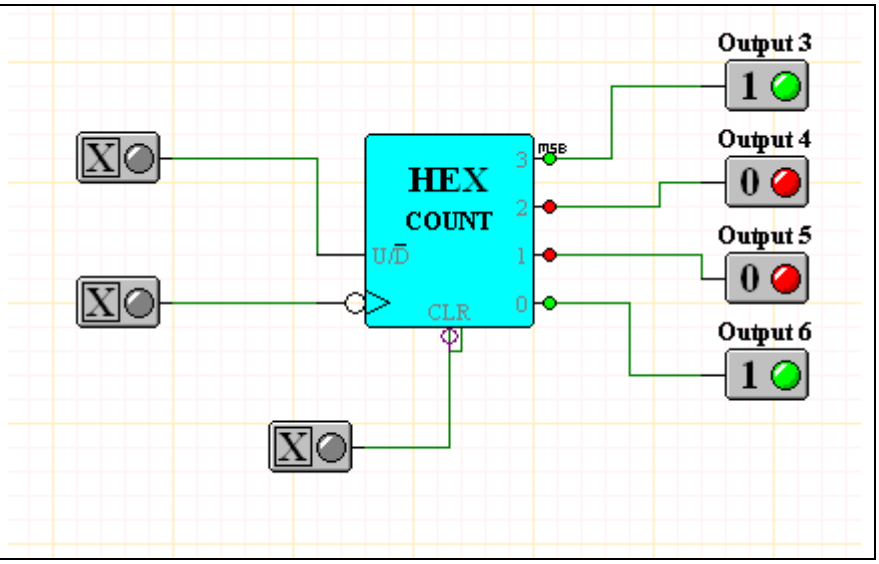
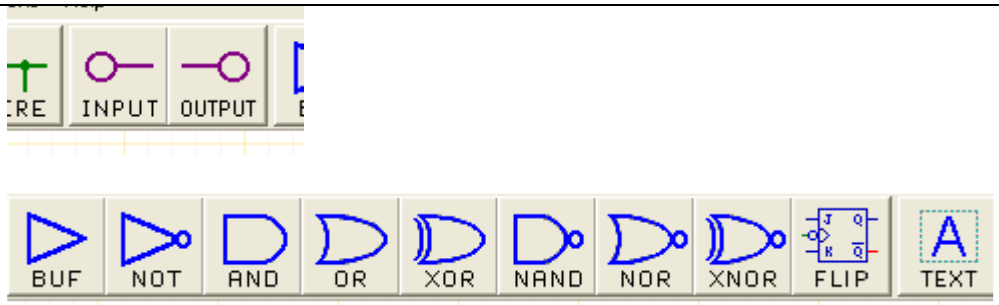
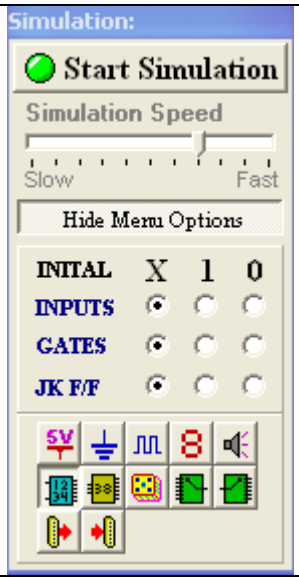
	For oven i skærmbilledet ses input og output-symboler, og de forskellige gates Og Flip Flop. .	
	Til højre kan vælges forskellige andre elektroniske enheder.	

WireDiagm

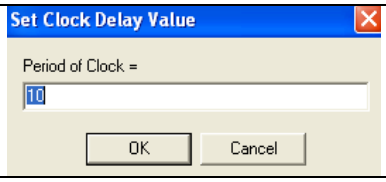
I denne del kan der tegnes diagrammer med forskellige 74xx komponenter.



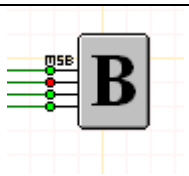
Nærmere beskrivelse af DigitalSim

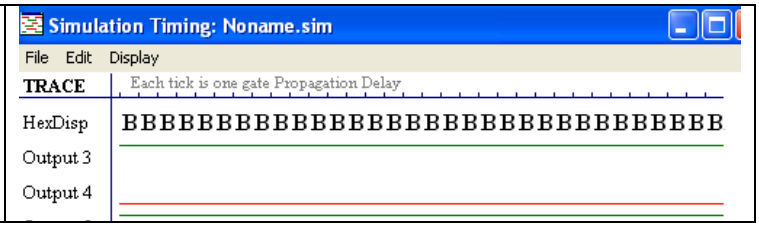
Eks. På et kredsløb:	
Input og output Og de forskellige gates.	
Til højre ses en boks, hvor man kan vælge forskellige elektroniske komponenter.	

Oscillator

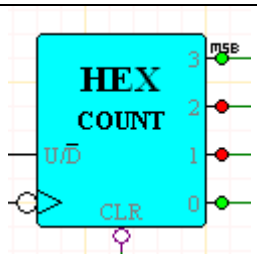


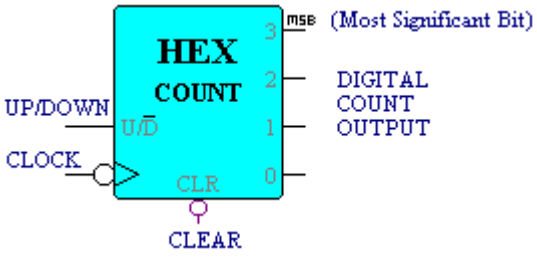
7-segment



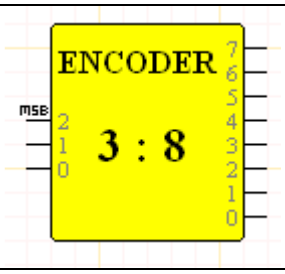


Counter

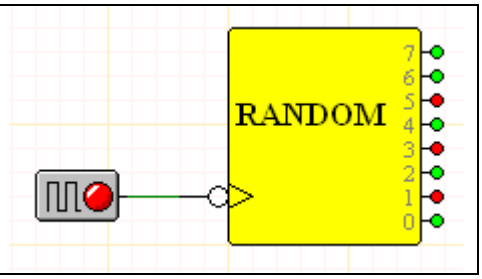




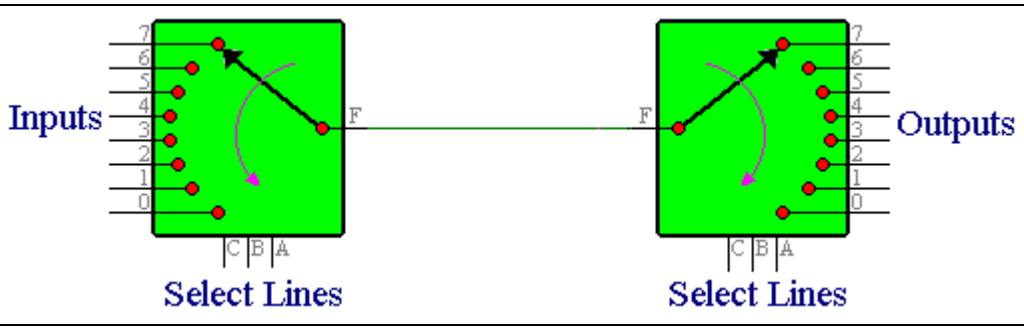
3 til 8 dekoder

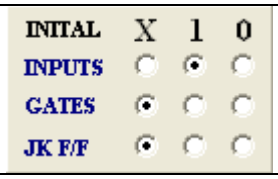


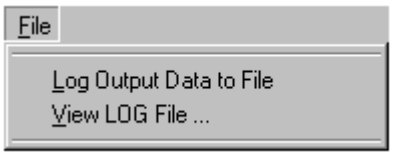
Tilfældigheds-generator



Multiplekser, Demultiple-xer



Inputs, initial spænding.			



Log data

Under en simulering ses et graf-vindue.